

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims:

1. (original) A semiconductor die package comprising;
a semiconductor die;
a leadframe having a chemically-etched surface; and
a capsule enclosing said die and at least a portion said leadframe.
2. (original) The semiconductor package of Claim 1 wherein said leadframe consists essentially of copper alloy.
- 3-6. (canceled)
7. (previously presented) A semiconductor package comprising:
a semiconductor die;
a leadframe having a chemically-etched surface; and
a capsule enclosing said die and at least a portion said leadframe;
said package further comprising an organo-metallic coating on the surface of the leadframe.
- 8-20. (canceled)
21. (previously presented) The semiconductor package of Claim 1 wherein the arithmetic mean deviation of a profile of said chemically-etched surface is in the range of 0.050 μm to 0.170 μm .
22. (previously presented) The semiconductor package of Claim 21 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 μm to 0.700 μm .
23. (previously presented) The semiconductor package of Claim 22 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μm to 1.500 μm .

24. (previously presented) The semiconductor package of Claim 21 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μm to 1.500 μm .

25. (previously presented) The semiconductor package of Claim 24 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm .

27. (previously presented) The semiconductor package of Claim 22 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm .

27. (previously presented) The semiconductor package of Claim 21 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm .

28. (previously presented) The semiconductor package of Claim 1 wherein the mean peak-to-valley height of said chemically-etched surface is in the range of 0.180 μm to 0.700 μm .

29. (previously presented) The semiconductor package of Claim 28 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μm to 1.500 μm .

30. (previously presented) The semiconductor package of Claim 29 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm .

31. (previously presented) The semiconductor package of Claim 28 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm .

32. (previously presented) The semiconductor package of Claim 1 wherein the ten-point height of irregularities of said chemically-etched surface is in the range of 0.400 μm to 1.500 μm .

33. (previously presented) The semiconductor package of Claim 32 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm .

34. (previously presented) The semiconductor package of Claim 1 wherein the maximum profile valley depth of said chemically-etched surface is in the range of 0.200 μm to 0.750 μm .

35. (previously presented) The semiconductor package of any one of Claims 21 to 34 further comprising an organo-metallic coating on the surface of the leadframe.